



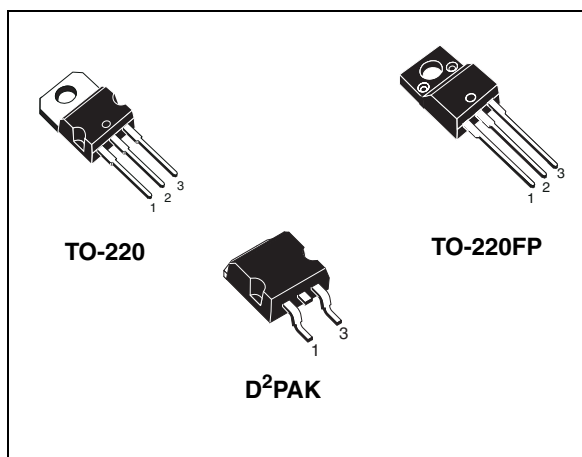
STB11NK40Z - STP11NK40ZFP STP11NK40Z

N-channel 400V - 0.49Ω - 9A TO-220 - TO-220FP - D²PAK
Zener-protected SuperMESH™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STB11NK40Z	400V	<0.55Ω	10A	110W
STP11NK40Z	400V	<0.55Ω	10A	110W
STP11NK40ZFP	400V	<0.55Ω	10A	30W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



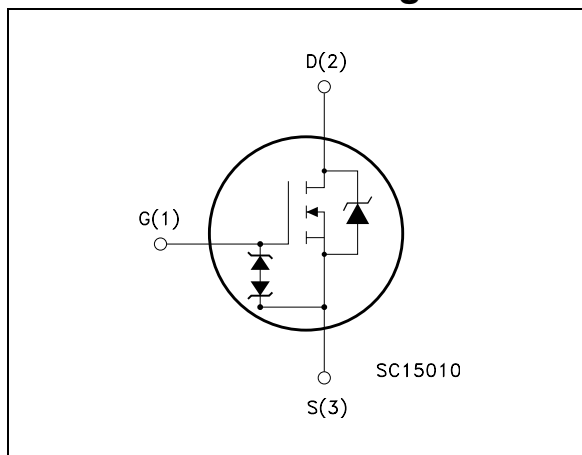
Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB11NK40ZT4	B11NK40Z	D ² PAK	Tape & reel
STP11NK40Z	P11NK40Z	TO-220	Tube
STP11NK40ZFP	P11NK40ZFP	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} = 0)	400		V
V _{DGR}	Drain-gate voltage (R _{GS} = 20kΩ)	400		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25°C	9	9 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100°C	5.67	5.67 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	36	36 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	110	30	W
	Derating Factor	0.88	0.24	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C= 100pF, R= 1.5kΩ)	3500		V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation withstand voltage (DC)	--	2500	V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 9A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	1.14	4.2	°C/W
R _{thj-a}	Thermal resistance junction-ambient max	62.5		°C/W
T _l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J Max)	9	A
E _{AS}	Single pulse avalanche energy (starting T _J =25°C, I _d =I _{ar} , V _{dd} =50V)	190	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	400			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V, V_{DS} = 0$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 4.5A$		0.49	0.55	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 4.5A$		5.8		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		930 140 30		pF pF pF
$C_{oss \text{ eq}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 320V$		78		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 320V, I_D = 9A$ $V_{GS} = 10V$ (see Figure 17)		32 6 18.5		nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%
2. $C_{oss \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD}=200\text{ V}$, $I_D=4.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 19)		20 20		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD}=200\text{ V}$, $I_D=4.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 19)		40 18		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD}=320\text{ V}$, $I_D=9\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 19)		15 17 30		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=9\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=45\text{ V}$, $T_j=150^\circ\text{C}$		225 1.6 14		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220 D²PAK

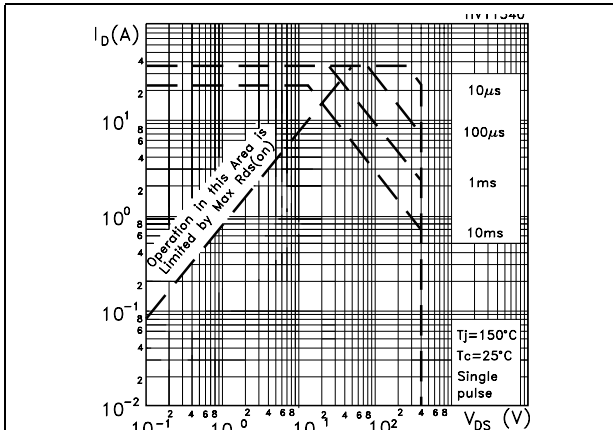


Figure 2. Thermal impedance for TO-220 D²PAK

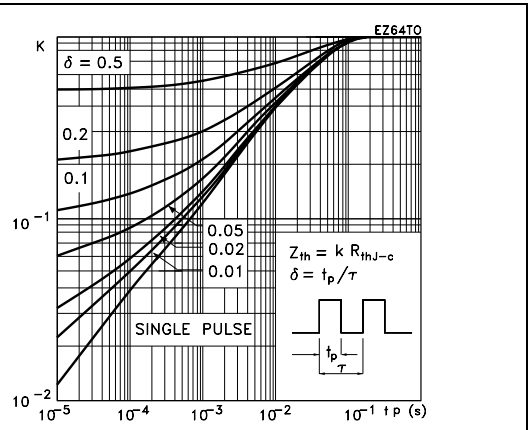


Figure 3. Safe operating area for TO-220FP

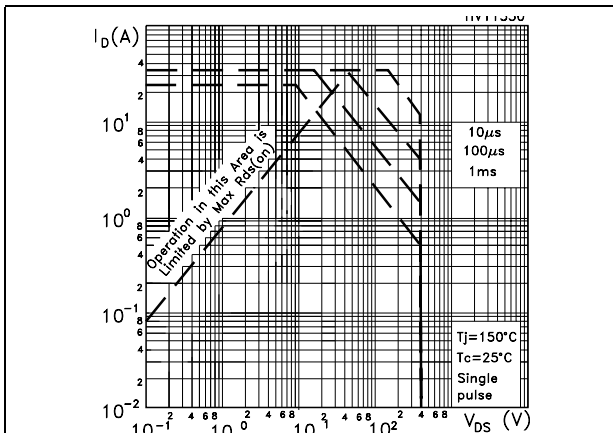


Figure 4. Thermal impedance for TO-220FP

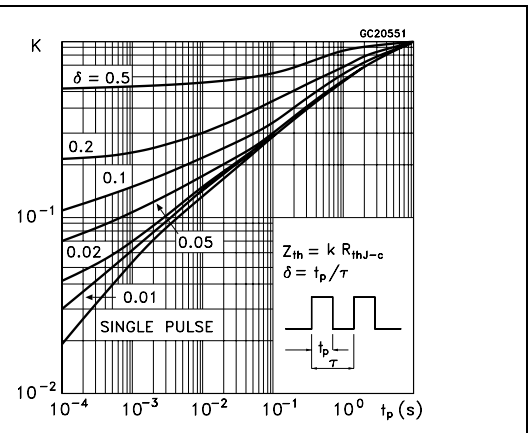


Figure 5. Output characteristics

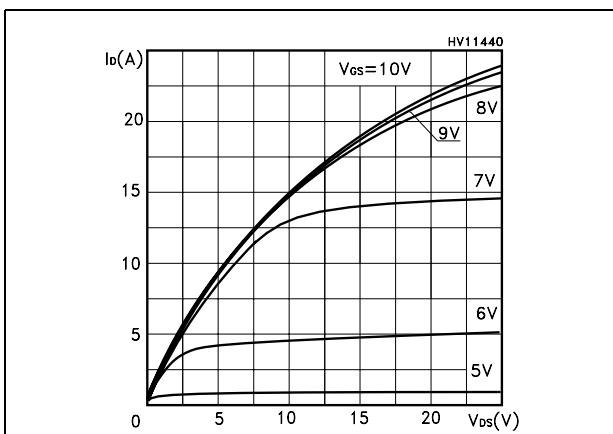


Figure 6. Transfer characteristics

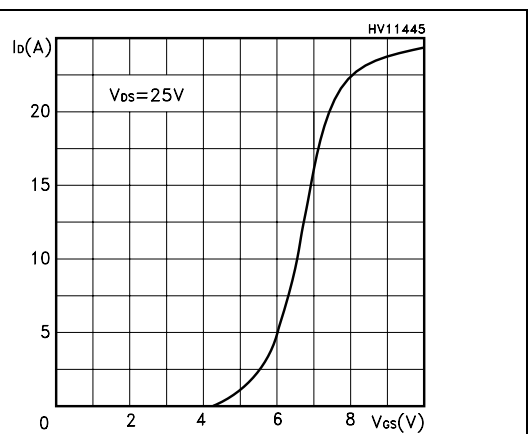


Figure 7. Transconductance

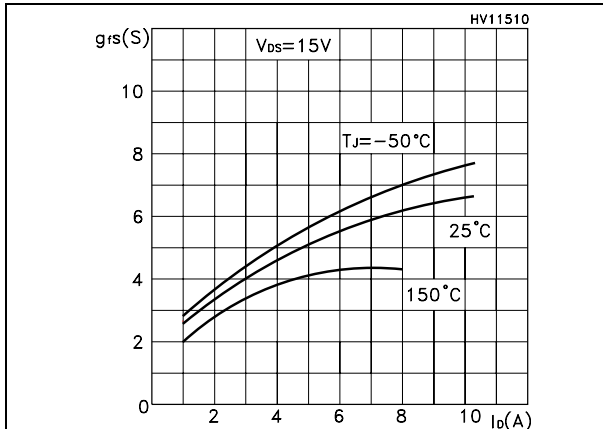


Figure 8. Static drain-source on resistance

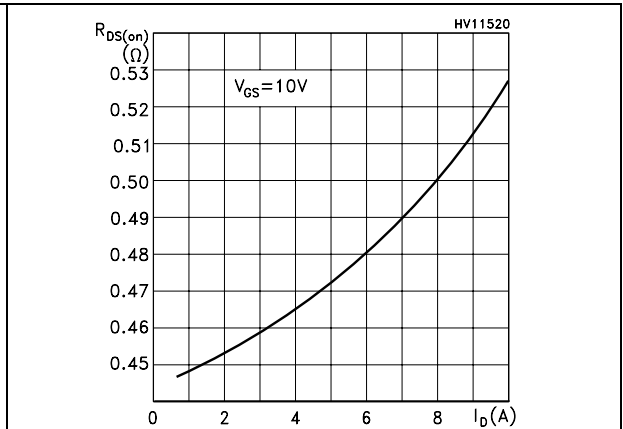


Figure 9. Gate charge vs gate-source voltage

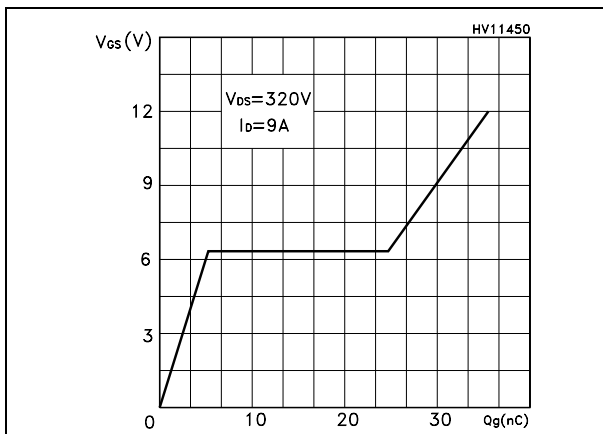


Figure 10. Capacitance variations

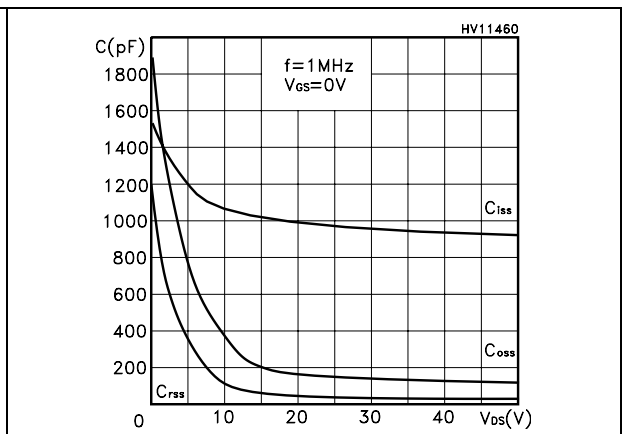


Figure 11. Normalized gate threshold voltage vs temperature

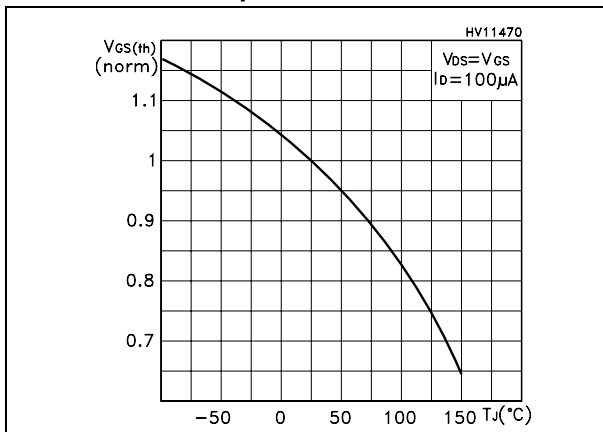


Figure 12. Normalized on resistance vs temperature

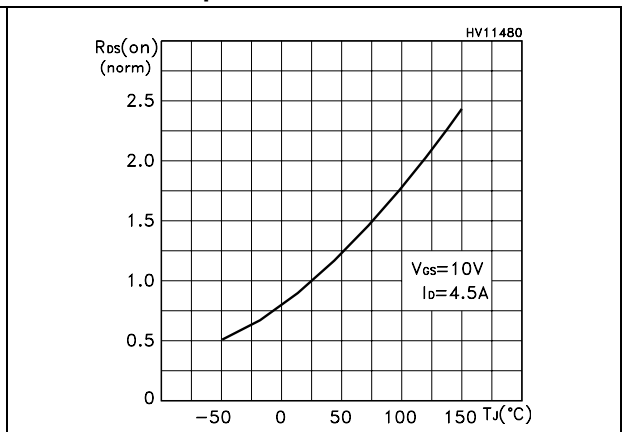


Figure 13. Source-drain diode forward characteristics

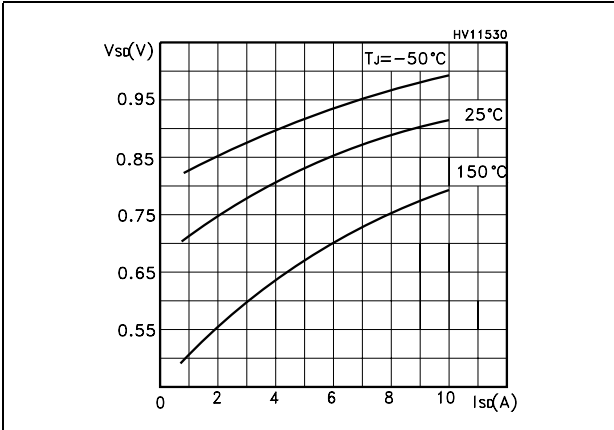


Figure 14. Normalized B_{VDSS} vs temperature

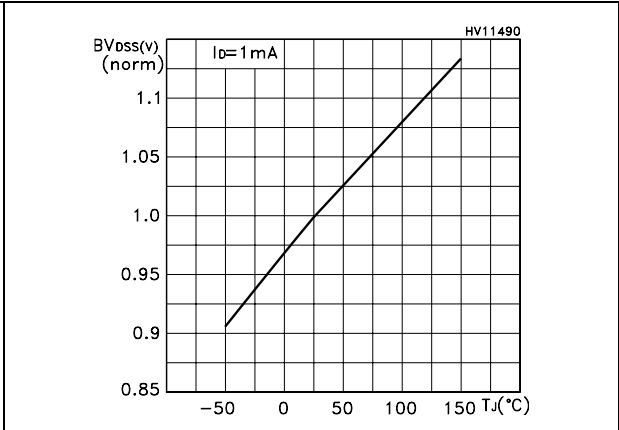
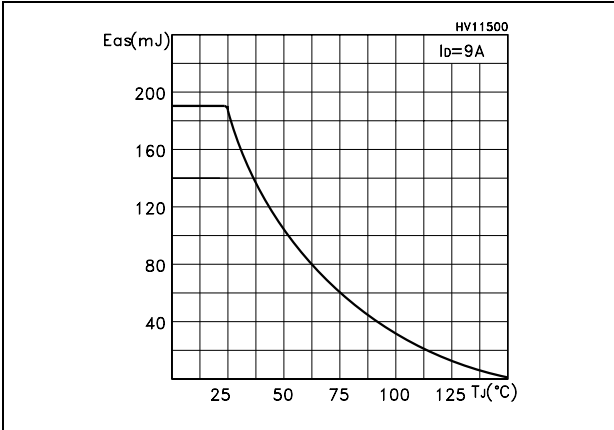


Figure 15. Maximum avalanche energy vs temperature



3 Test circuit

Figure 16. Switching times test circuit for resistive load

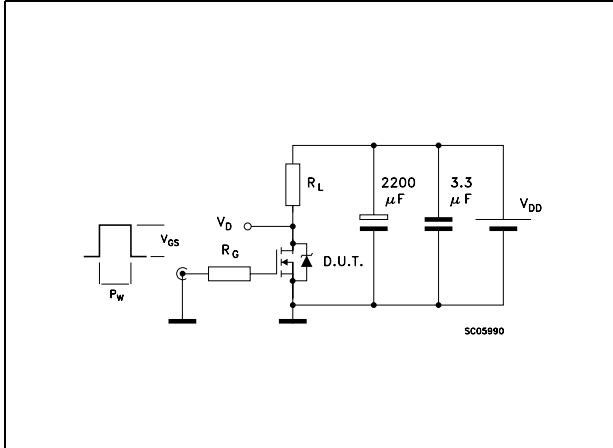


Figure 17. Gate charge test circuit



Figure 18. Test circuit for inductive load switching and diode recovery times



Figure 19. Unclamped Inductive load test circuit



Figure 20. Unclamped inductive waveform



Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

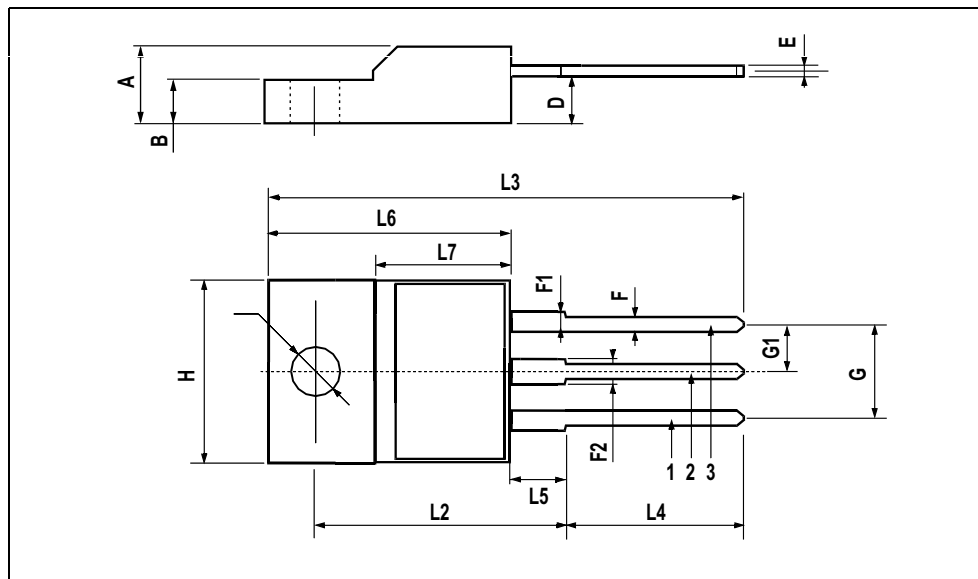
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



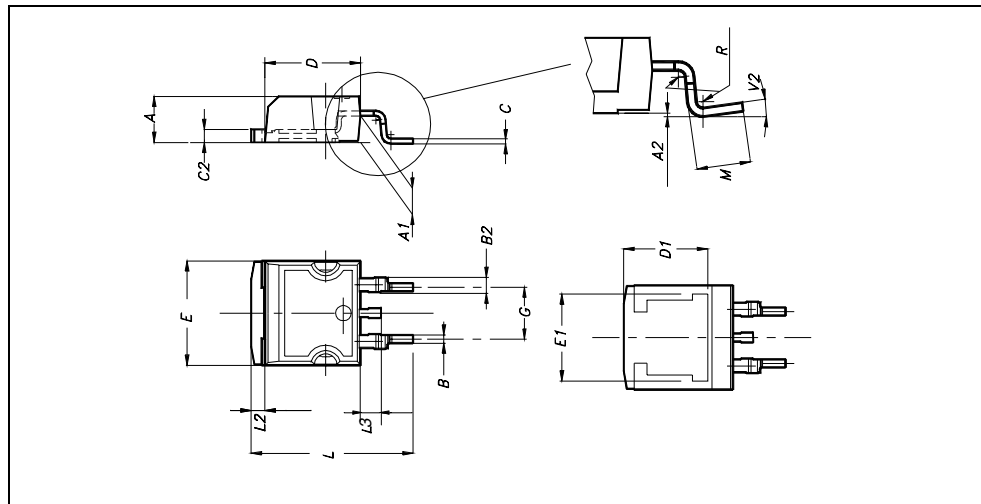
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

* on sales type

6 Revision history

Table 9. Revision history

Date	Revision	Changes
23-Aug-2005	2	Preliminary version
28-Oct-2005	3	Complete version
26-Jul-2006	4	New template, no content change
22-Nov-2006	5	Corrected unit on Table 4.: On/off states
18-Jan-2007	6	Typo mistakes on page 1

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